# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | Frankie F. Roohparvar | Examiner: Trong Q. Phan | |
| Serial No.: | 09/608,580 | Group Art Unit: 2818 | |
| Filed: | June 30, 2000 | Docket: 400.006US01 | |
| Title: | ZERO LATENCY-ZERO TURNAROUND SYNCHRONOUS FLASH MEMORY | | |



## AMENDMENT AND RESPONSE

Commissioner for Patents
BOX NON-FEE AMENDMENT
Washington, D.C. 20231

In response to the Office Action dated January 8, 2002, please consider the following remarks:

## IN THE SPECIFICATION

Please amend the first paragraph on page 42 as follows:

A data buffer 330 can be coupled to the data communication connections to manage the bi-directional data communication. This buffer can be a traditional FIFO or pipelined input/output buffer circuit. The write latch is coupled between the data buffer and the memory array to latch data provided on the data communication connections. Finally, a control circuit 340 is provided to manage the read and write operations performed on the array.

## IN THE CLAIMS

8. The method of claim 6 further comprises:

receiving a row address on a first clock cycle;

receiving a column address on a second clock cycle following the first clock cycle, wherein the write data is received on the data connections on the second clock cycle.